**A Common Boolean Logic(CBL) implementation for modified CSLA**

**Ahstract**

This project deals with the comparison of the VLSI design of the carry look-ahead adder (CLAA) based 32-bit unsigned integer multiplier and the VLSI design of the carry select adder (CSLA) based 32-bit unsigned integer multiplier. Both the VLSI design of multiplier multiplies two 32-bit unsigned integer values and gives a product term of 64-bit values. The CLAA based multiplier uses the delay some time for performing multiplication operation where as in CSLA based multiplier also uses nearly the same delay time for multiplication operation. But the area needed for CLAA multiplier is reduced to 31 % by the CSLA based multiplier to complete the multiplication operation. These multipliers are implemented using Xilinx ise ,simulation diagrams are viewed through Modelsim tool.

**Software used :**

Modelsim simulator

Xilinx

**Language:**

Verilog HDL/VHDL